CHAPTER 4. I/O CARDS

Output Cards (L)	60, 60A, 62, 67
Input Cards (M)	61, 87
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Transmitter and Receiver	C62B, C61
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Line Receiver	E13
Line Driver	E15
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Receiver	H11A
Transmitter	H19
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Transmitter and Receiver	P14C, P16A

OUTPUT CARDS (L)

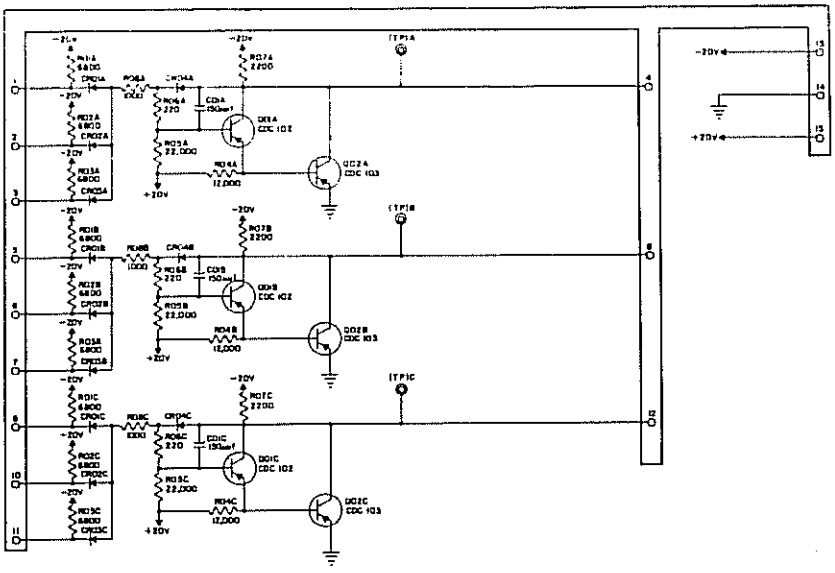
Card Types 60, 60A, 62 and 67

The circuits contained on these cards adapt the relatively low level 1604 logic voltages to the relatively high level voltages necessary for transmission over a 1604-type I/O cable. Each card contains three separate circuits designated A, B, and C.

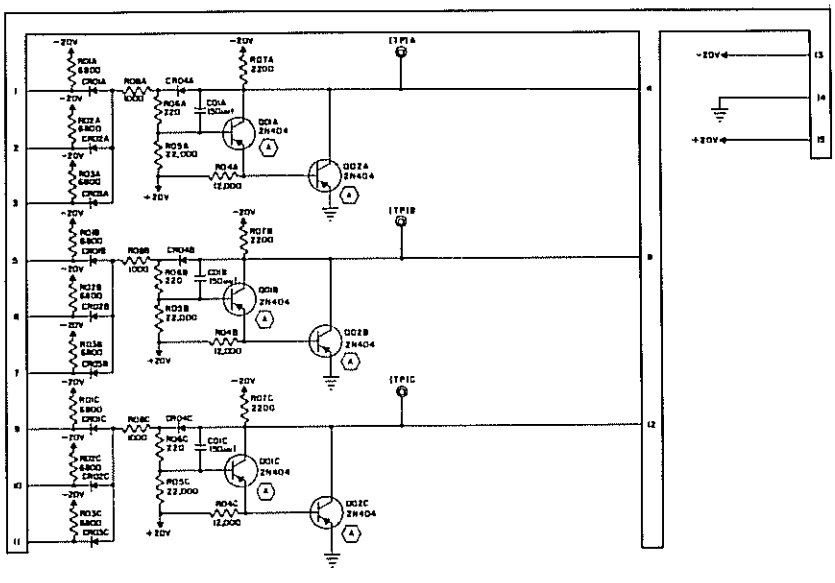
These circuits are similar to 1604-type inverters, in that they contain a common emitter transistor circuit producing a 180^{o} electrical phase shift

The switching speed of the circuit is limited by the 150 uuf of Miller feedback capacitance, and the feedback network allows a -0.5v "0" input to drive the circuit to cutoff. Input and output levels are as follows:

Input	Output
-3v "1"	-0.5v
-0.5v "0"	-18v



Output 60



Output 60A

INPUT CARDS (M)

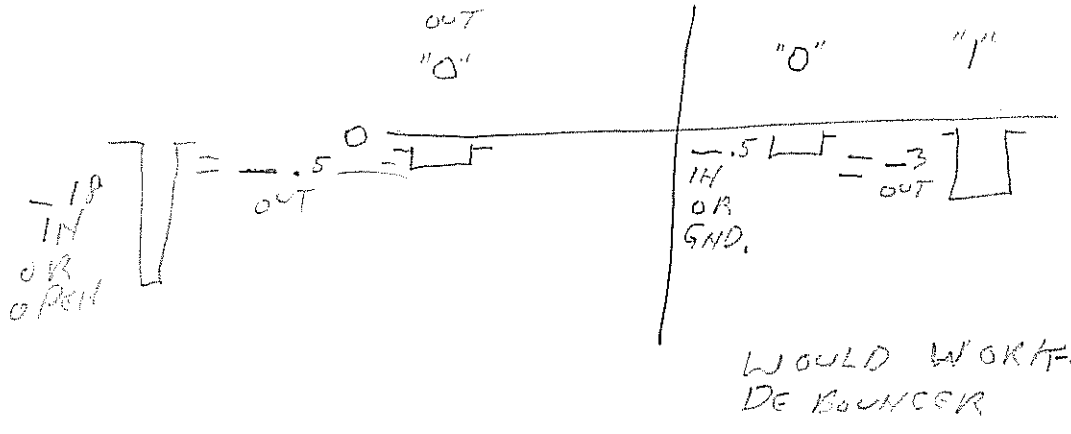
Card Types 61 and 87

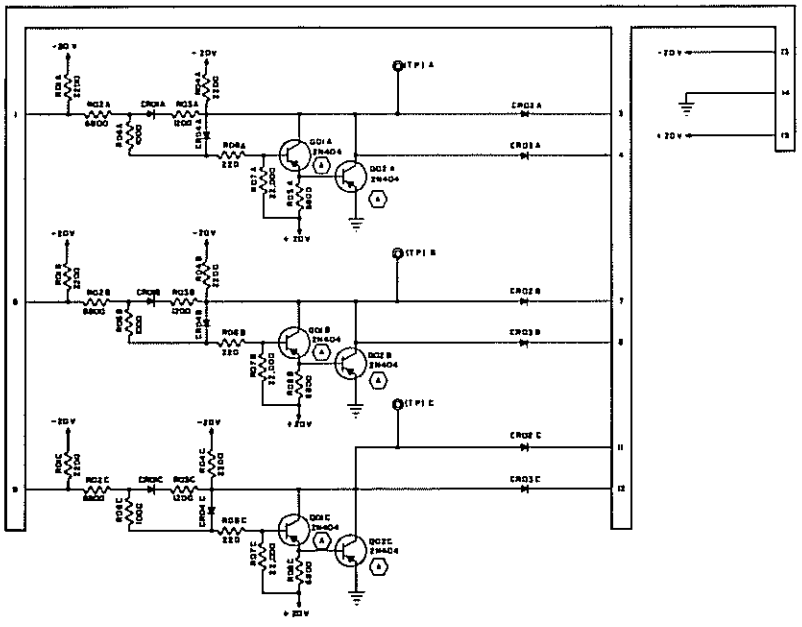
The circuits contained on these cards adapt relatively high line voltage used for 1604-type cable transmission to the relatively low-level voltage used for logical functions. Each card contains three separate circuits designated A, B, and C.

These circuits are similar to the 1604-type inverter, except that the modified input allows the circuit to accept higher voltage signals.

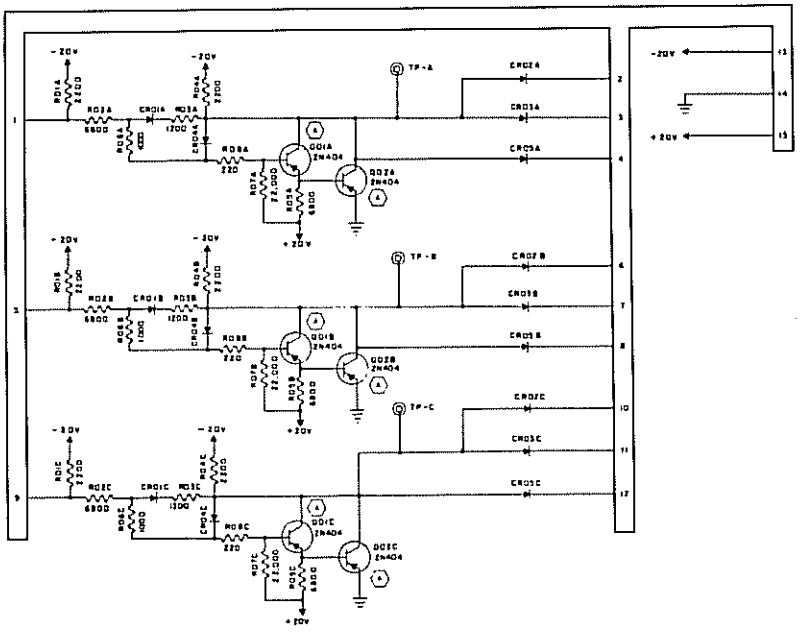
Inputs and outputs are as follows:

Input	Output
-0.5v (or ground)	-3v "1"
-18v (or open)	-0.5v "0"

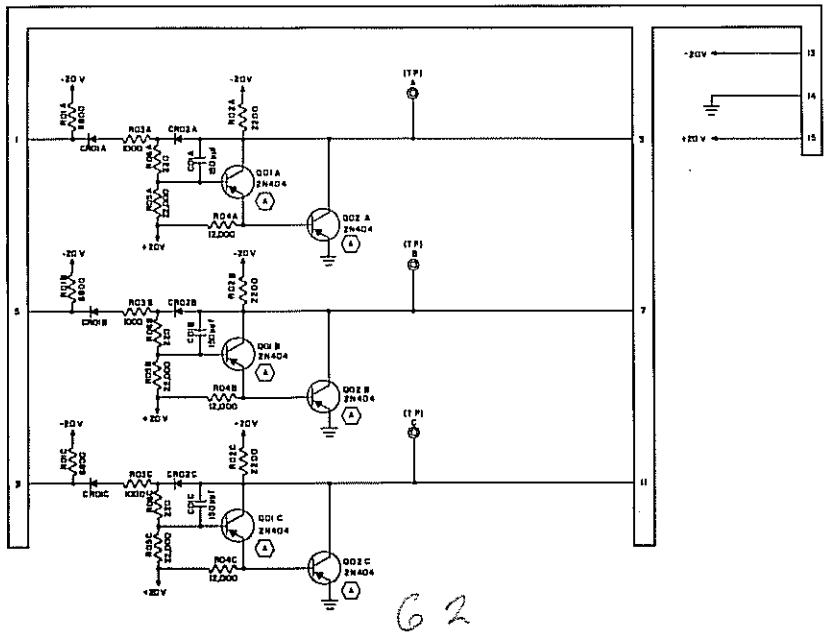




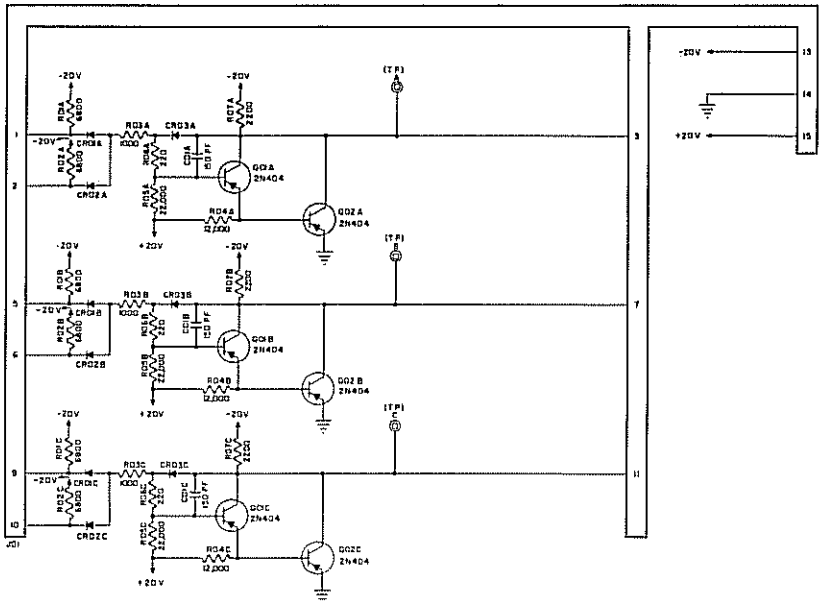
Input 61



Input 87


-20V
+20V
(TP) A
(TP) B
(TP) C
Q01A 2N404
Q02A 2N404
Q01B 2N404
Q02B 2N404
Q01C 2N404
Q02C 2N404

62

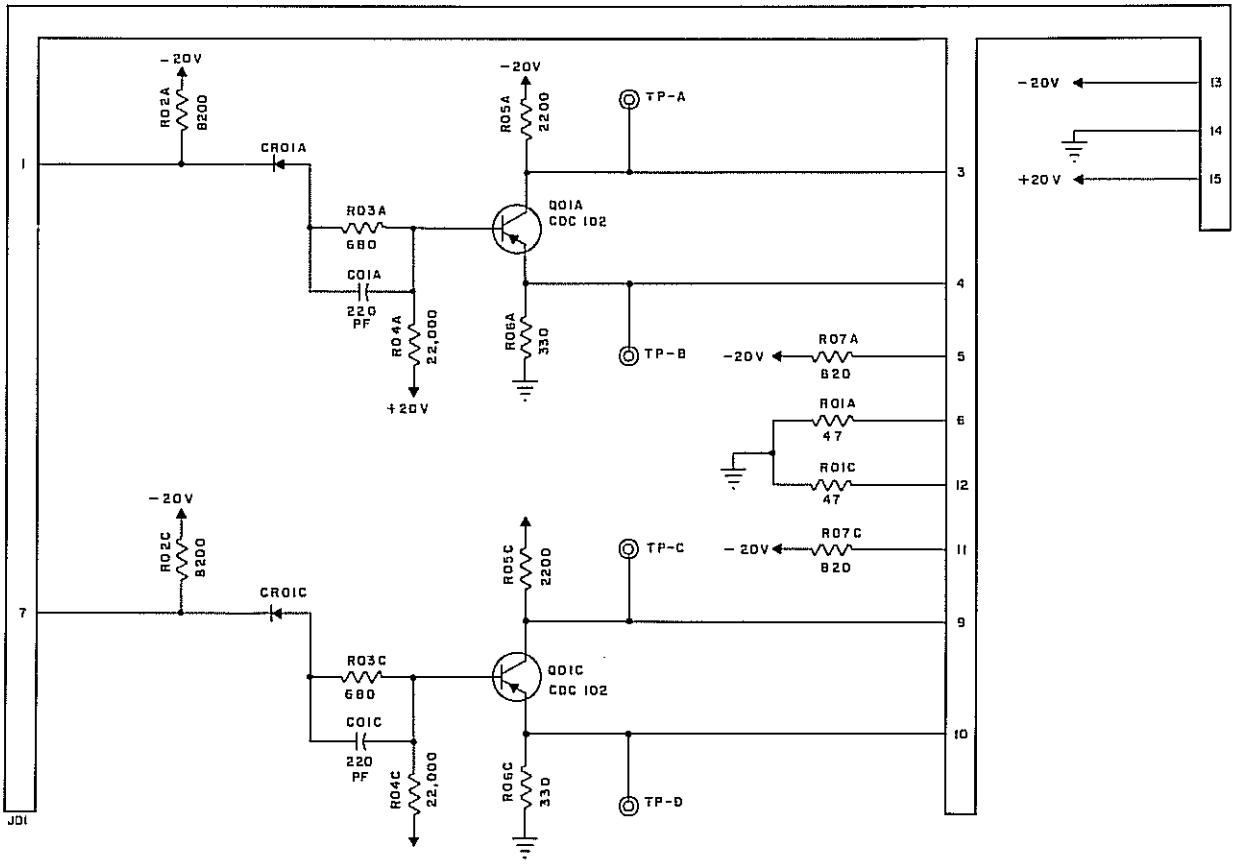

-20V
+20V
(TP) A
(TP) B
(TP) C
Q01A 2N404
Q02A 2N404
Q01B 2N404
Q02B 2N404
Q01C 2N404
Q02C 2N404

Output 67

OUTPUT

Card Type 79A

The function of the circuits on this card is to enable 1604-type logic to interface with IBM equipment. The card contains a biasing network, and both "P" and "N" signal levels may be produced as shown in the accompanying diagram.



Output 79A

TRANSMITTER AND RECEIVER
Card Types C62B and C61

GENERAL

The circuit configuration shown on page 4-C62-3 performs high speed transmission of digital information from one module to another. Inputs to the transmitter circuit are logical "1's" and "0's" of -5.8v and -1.1v, respectively. The transmitter converts these single-ended inputs to double-ended outputs suitable for transmission over a balanced transmission line. Tests using an 8-megacycle bit rate input have shown that 1 transmitter satisfactorily drives 20 receivers and 19 unused transmitters located at any point along a 200 foot transmission line.

The transmission line is twisted-pair having a characteristic surge impedance of approximately 110 ohms and is terminated at each end in its characteristic impedance. Transmission signal levels are approximately 0.5v line-to-line, and a "1" is distinguished from a "0" by a full voltage reversal.

The line voltage levels which represent a "0" are established by current flow from the +20v to the -20v source at the terminating resistors. Each of these currents is of the order of 5 ma, so that the total voltage developed across the terminating resistors is approximately 0.5v.

When the 3-way AND input to the transmitter is disabled by a "0", transistor Q01 is turned on and current is shunted around the two constant current drivers Q02 and Q03. With the AND enabled by "1" inputs, Q01 is turned off, thus allowing Q02 and Q03 to drive a constant 20 ma into the transmission line. Originally, the bias networks on the line were producing a 5 ma current flow in one direction through the terminating resistors, but when the transmitter switches on, the direction of net current flow through the terminating resistors effectively reverses. The current from the transmitter divides into two 10 ma currents which flow through each line termination. This current is in the opposite direction to the 5 ma bias current; thus the net current flow is 5 ma in the opposite direction, producing a voltage drop equal and opposite to the original voltage. This results in a full voltage reversal for separating a "1" from a "0", although the signal level remains of the order of 0.5v line-to-line.

TRANSMITTER, Card Type C62

The printed circuit card contains two identical transmitter circuits designated A and B. A typical circuit is shown on page 4-C62-3.

The logic input circuitry consists of a 3-way AND. The output of a standard logic card constitutes a proper input to a transmitter. A logical "1" input causes transistor Q01 to turn off and Q02 and Q03 to turn on, while a "0" input has the opposite effect.

A -1. 1v "0" input causes the emitter-base junction of Q01 to be forward biased, fully turning on Q01. When Q01 is turned on, a shunt path for current is provided around Q02 and Q03. Since Q02 and Q03 no longer have a source of current, no current is injected into the transmission line.

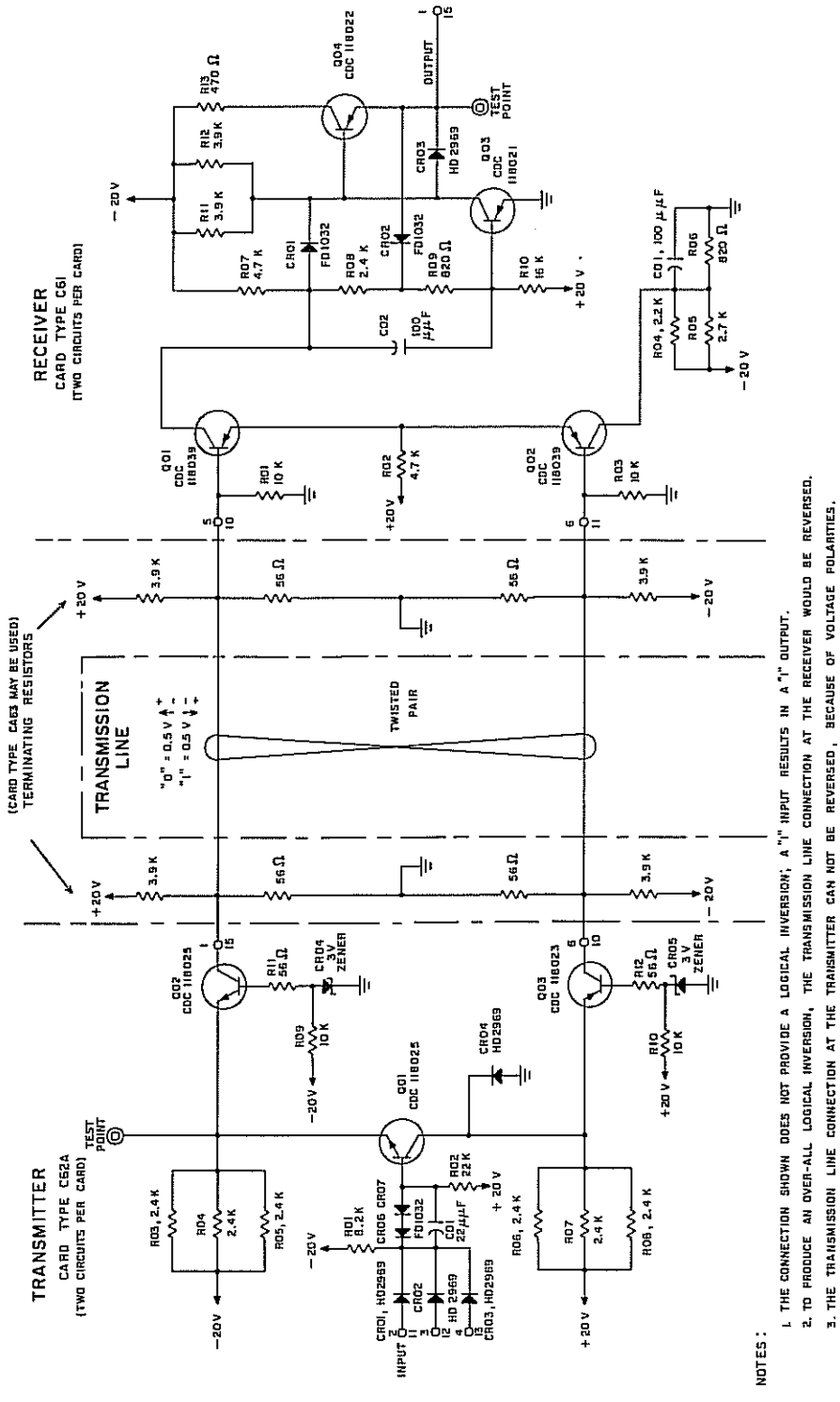
When the AND input is satisfied, the base of Q01 is held at approximately -5 volts. This reverse biases the emitter-base junction by approximately 3 volts and causes Q01 to be turned off. Since the shunt path for current around Q02 and Q03 no longer exists, they become constant current generators of opposite polarities. Q03 injects a current of approximately 20 ma into the line and a like amount of current flows out of the line into Q02.

The base networks of Q02 and Q03 each contain a 3v zener diode which performs two functions. In the first case, the zener diode sets the voltage level at which the emitters of Q02 and Q03 reach their turned-on state. This, in turn, sets the threshold that must be overcome at the base of Q01, since its emitter is at the same potential as the emitter of Q02. In the second case, the zener diodes set the base voltages of Q02 and Q03 which determine how much noise voltage is allowed at the collectors before the collector-base junctions become forward biased. This value of noise voltage is something over 3 volts since the forward drop of the collector-base junctions adds to the zener diode voltage. This means that the transmitter operates satisfactorily with up to 3 volts of random noise on the transmission line.

The transmitter must be connected to the line in only one polarity, as shown on page 4-C62-3. This is necessary to provide current through the terminating resistors in a direction opposite the bias current.

TRANSMISSION LINE

A terminated balanced twisted-pair transmission line carries digital information from the transmitter to the receiver. This information is in the form of line-to-line



Transmitter and Receiver C62 and C61

differential voltages of the order of 0.5v, with a complete voltage reversal distinguishing a "1" from a "0".

The surge impedance of the transmission line is 100 to 120 ohms. The line is terminated at each end with a 112-ohm resistive load, consisting of two 56-ohm resistors in series across the line with an optional center ground reference. This provides very good impedance matching and, as a result, reflections and standing waves are minimized.

The line is biased at each end by means of 3.9k resistors to +20v and -20v to achieve a 5 ma bias current through the terminating resistors. This holds the "0" state signal level at 0.5v line-to-line.

The length of a transmission line may be up to 200 feet, with as many as 20 transmitters and 20 receivers placed in parallel along its length.

Bit rates of 8 mc or greater are possible on a 200 foot line. Low bit rates over longer distances are limited by the d-c line losses; however transmitters may be paralleled for longer distances to overcome these losses.

The velocity of signal propagation along the line is approximately 50 percent to 60 percent of the velocity of light. This results in a time delay per foot of the order of 1.6 to 1.8 nanoseconds.

The balanced system using differential receiving techniques allows a difference in noise levels up to 3v to be tolerated between the transmitter ground reference and the receiver ground reference.

RECEIVER, Card Type C61

The printed circuit card contains two identical receiver circuits designated A and B. A Typical example is presented on page 4-C62-3. This portion of the circuit connected to the collector of Q01 is similar to a logical inverter, which is discussed elsewhere in this report.

This circuit functions as both a differential amplifier and a discriminator. It provides a logic output of either "1" or "0", according to the polarity of the differential 0.5v signal which the two input terminals receive from the transmission line.

The circuit inputs are connected directly into the bases of Q01 and Q02. The 0.5v differential input is centered about ground, so one input shifts approximately 0.25v positive while the other input shifts negative a similar amount. The two input transistors Q01 and Q02 are PNP type CDC C07's; thus the transistor which receives the negative input conducts more heavily while the one receiving the positive input conducts less heavily.

The circuit is such that a negative input to the base of Q01 and a positive input to the base of Q02 results in a logical "1" at the receiver output. Under the opposite conditions of a positive input to Q01 and a negative input to Q02, the output is a logical "0". Thus, by reversing the connections at the receiver inputs, it is possible for a given set of conditions on the transmission line to produce either a "1" or a "0" at the receiver output.

The circuit shown on page 4-C62-3 does not produce an inversion between input to the transmitter and output from the receiver. A "1" input to the transmitter produces a transmission line signal of approximately 0.5v line-to-line with the polarity as shown. This allows transistor Q01 to apply approximately 5 ma of collector current to the junction of R07, R08, and the anode of CR01, which causes Q03 to switch off and Q04 to switch on, providing a "1" output. In this state, transistor Q04 can drive 8 OR loads. With opposite conditions at the receiver input, the output can drive 8 AND loads.

GROUND RULES

1. The output of a logic card constitutes a proper input to a transmitter.
2. The output of a receiver constitutes a proper input to a logic card.
3. A receiver may drive 8 OR loads, 8 AND loads, or any combination resulting in 8 loads total.
4. The transmission line is twisted-pair, having a surge impedance of 100 to 120 ohms.
5. The transmission line may be any length up to 200 feet.
6. The transmission line is terminated at each end in a resistive load approximately equal to its surge impedance.
7. A logical inversion between input to transmitter and output from receiver may or may not occur, depending upon the transmission line connections at the receiver.
8. The transmission line connections at the transmitter can not be reversed, due to the polarity of the line bias voltage.

9. Up to 20 transmitters and 20 receivers may be connected along a transmission line.
10. A transmitter having an 8 megacycle bit rate input will drive 20 receivers at the end of a 200 foot transmission line, with 19 inactive transmitters also connected to the line.
11. Inactive transmitters and receivers do not load a transmission line and do not have to be disconnected from it.
12. No more than 8 transmitters should be driven by an inverter and no more than 7 should be driven by a flip-flop.

MODIFIED M^{---} INPUT
Card Types C75* and C75B

FUNCTION

This card contains two identical circuits. Its function is to enable the 3600 computer system to receive information from a 1604 type input/output cable. This is done by converting the "1" and "0" signal levels from -0.7v and -18v to -5.8v and -1.1v, respectively.

OPERATION

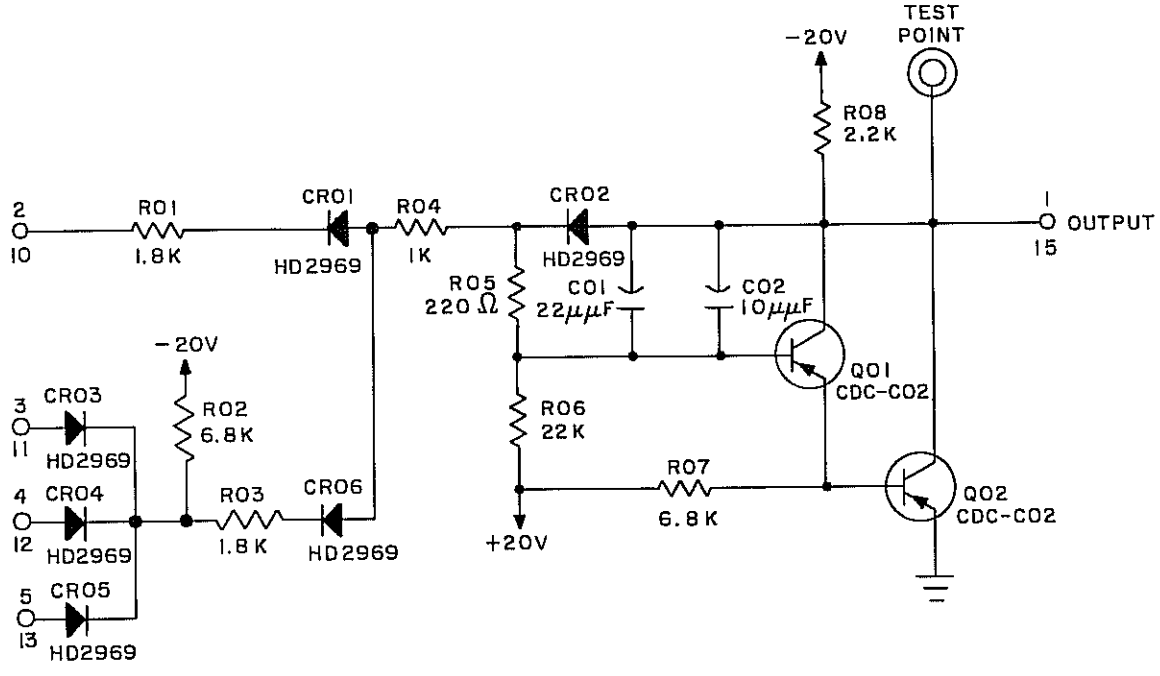
This circuit is essentially a single inverter having one OR input which has been modifie by the deletion of the input coupling capacitor and the addition of resistors R01 and R02. These provide a voltage dividing effect, so a -18v input results in approximately -6v at the cathode of CR01. Similarly, a -0.7v input results in -0.7v at that point.

The remainder of the circuit is identical to a single inverter, which is discussed elsewhere.

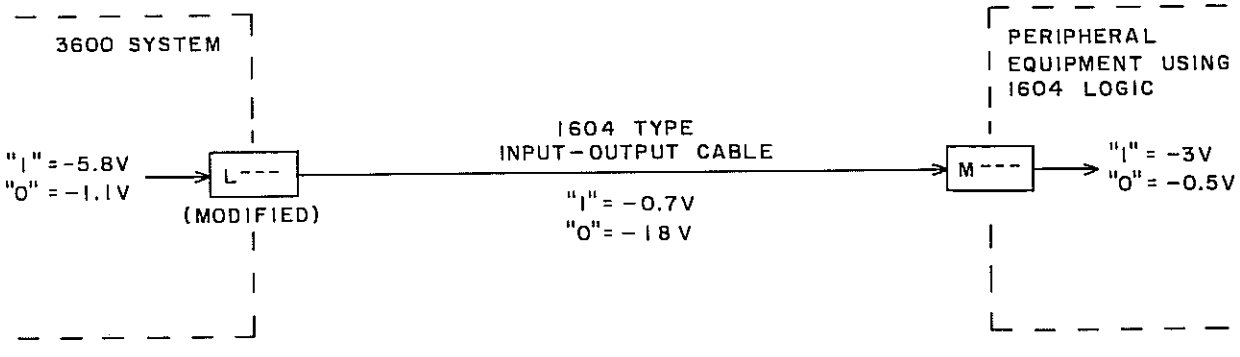
The C75B is capable of driving 8 OR loads, 8 AND loads, or any combination resulting in 8 loads total.

The C75 is capable of driving 3 OR loads, 8 AND loads, or any combination resulting in 8 loads total, but not to exceed a total of 3 OR loads.

*All future cards of this type are C75B.



TYPICAL INSTALLATION



Modified L--- Output C76
(Two circuits per card)

Transistor Q01 is connected as an emitter follower and Q02 as a grounded emitter stage. Thus when Q01 switches on, Q02 conducts heavily, providing a low impedance path from ground to the circuit output. The transistors are clamped out of saturation by diode CR02, but their collector potential is approximately -0.7v when both are in the conduction state.

A positive-going input causes transistor drive current to decrease, and when the input becomes more positive than -3v, transistor Q02 switches off, and the circuit output approaches -18v.

The switching time of the circuit is approximately 0.8 usec. The limiting factor is the 32 uuf of Miller feedback capacitance, which effectively slows the response of Q01.

LONG LINE DRIVER AND RECEIVER
Card Types CA98 and HA26

GENERAL

This circuit configuration performs high-speed transmission of digital information from one module to another over distances to 1000 feet. The driver card converts system logic levels into voltages suitable for output over an unbalanced transmission line. The receiver card converts the transmission line voltages into system logic levels capable of operating subsequent logical stages.

Transmitted carrier levels are -0.15v for a logic "1" and -2.1v for a logic "0". These levels are established by current flow through the termination networks. When the transmitter is turned off, the terminating network biases the line at 2.1v while turning on the long line driver forces the line to the -0.15v level.

LONG LINE DRIVER, Card Type CA98

The printed circuit card shown in the illustration contains two identical transmitter circuits which are designated A and B.

The logic input circuitry consists of a 3-way AND and an OR input. A -1.1v logic "0" results in the application of a positive potential to the base of Q01. Consequent emitter follower action causes a positive voltage to be coupled to the base of Q02. The resultant reverse bias condition at the emitter/base junction turns off Q02.

When Q02 is turned off, the transmission line will be biased at -2.1v. A -5.8v logic "1" signal causes a negative potential to be applied to the base of Q01. The resultant current increase in Q01 allows the base current of Q02 to increase to the saturation level. The saturation of Q02 forces the transmission line to the -0.15v level.

TRANSMISSION LINE

A terminated unbalanced transmission line conveys digital information between the driver and receiver cards. A -2.1v input to the receiver card signifies a logic "0" while a -0.15v level signifies a logic "1".

The line is terminated at each end in approximately 110 ohms. A normal -2.1v line level is established by the terminating network, while turning on the driver forces the line to -0.15v.

Separate power supplies may be used with each terminating network. The two power supplies are interconnected by means of the illustrated diode network. This arrangement gives either or both power supplies the ability to bias the line.

The transmission line, which is limited to 1000 feet, can service combinations of up to eight long line drivers and eight long line receivers.

Two electrically paralleled connectors connect a given piece of equipment to the transmission line. Equipment located at the extremities of the line must have one of its connectors directed to a termination network.

The velocity of signal propagation along the line is approximately 50 to 60 percent of the velocity of light. The resultant time delay per foot is of the order of 1.6 to 2.0 nanoseconds.

The long line driver/receiver will tolerate typical noise levels to 0.75v.

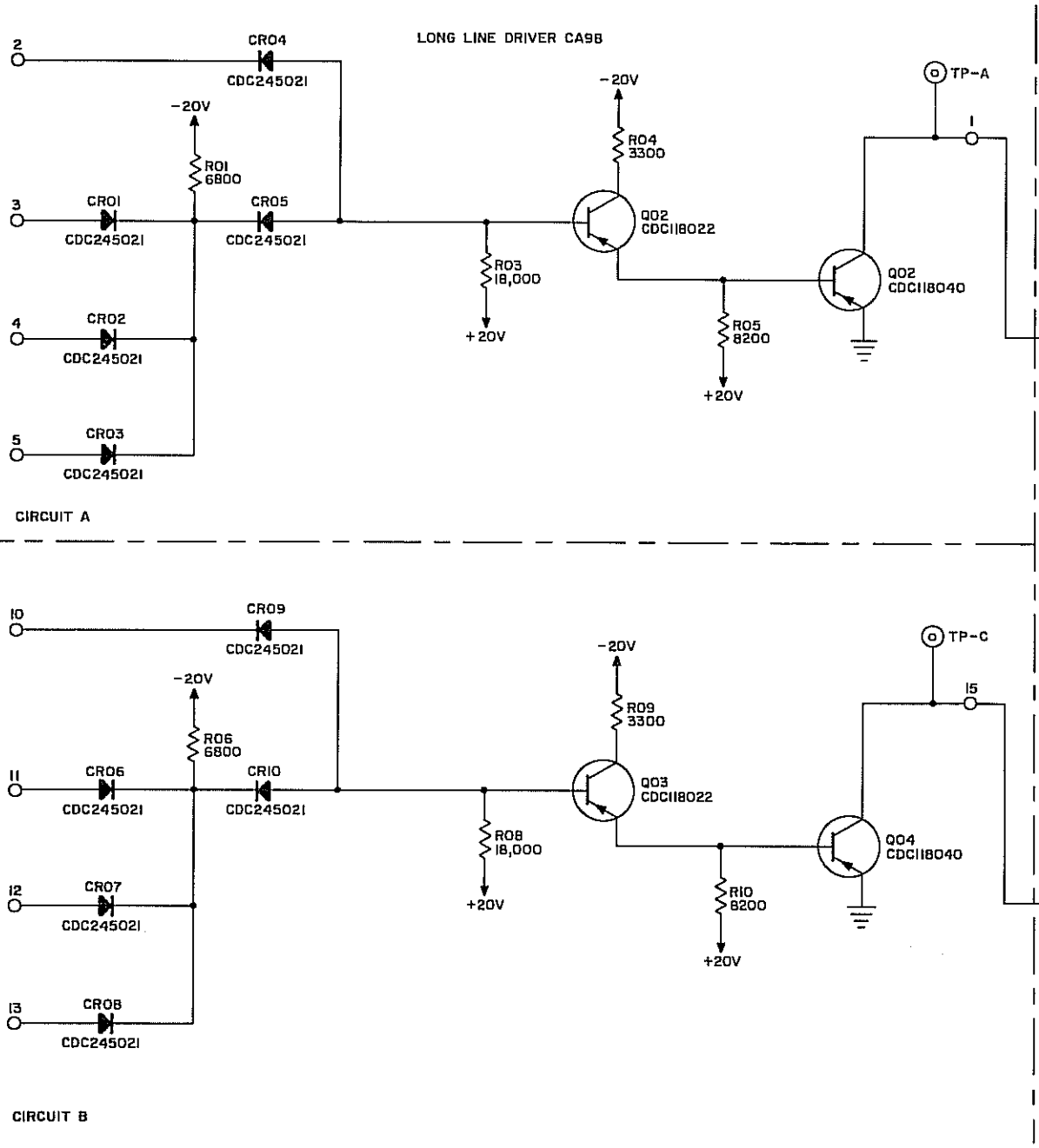
LONG LINE RECEIVER, Card Type HA26

This card contains two identical long line receiver circuits designated A and B. The receiver card responds to transmission line inputs of -2.1v and -0.15v which signify logic "0" and logic "1" inputs respectively. A -2.1v signal at the receiver input is applied to the base of Q01. The resultant forward bias condition allows conduction through Q01. Emitter follower action forward biases Q02. The resultant saturation of Q02 forces the collector potential to 0.2v.

A -0.15 signal at the receiver input turns Q01 off. This allows diode CR01 to become forward biased permitting feedback between the base and collector. This feedback stabilizes the collector voltage at -5.8v.

GROUND RULES

1) The output of a logic card constitutes a proper input to a long line driver.
2) The output of a long line receiver constitutes a proper input to a logic card.
3) A long line receiver may drive up to eight "AND" loads or up to three "OR" loads.
4) The transmission line may be of any length to 1000 feet. Transmission lines over 500 feet in length use 20-gauge wire, whereas lines less than 500 feet may use 24-gauge wire.
5) Any combination of up to eight long line drivers and eight long line receivers may be connected to one transmission line.


LONG LINE DRIVER CA98
2
CR04
CDC245021
-20V
R01
6800
3
CR01
CDC245021
CR05
CDC245021
4
CR02
CDC245021
5
CR03
CDC245021
R03
18,000
+20V
-20V
R04
3300
Q02
CDCII8022
R05
8200
+20V
TP-A
1
Q02
CDCII8040
CIRCUIT A
10
CR09
CDC245021
-20V
R06
6800
11
CR06
CDC245021
CR10
CDC245021
12
CR07
CDC245021
13
CR08
CDC245021
R08
18,000
+20V
-20V
R09
3300
Q03
CDCII8022
R10
8200
+20V
TP-C
15
Q04
CDCII8040
CIRCUIT B